

REMARKS

Allowance of claims 33-40 and the indication that claim 32 would be allowable in independent form is noted with appreciation. It is respectfully submitted that all claims are allowable for the reasons which follow.

Claims 23-31 were rejected under 35 U.S.C. 102 over Yoshii. This rejection is respectfully traversed.

The Yoshii patent discloses a monolithic ceramic electronic component composed of a monolithic ceramic element containing internal electrodes and a pair of external electrodes. The external electrodes do have a three layer structure but that structure is very different from that claimed in the present application.

Each of the external electrodes 14 and 16 contain an innermost layer (142, 162), and intermediate layer (144, 164) and an exterior layer (146, 166_). The outmost layers contain different conductive materials and different glasses while the intermediate layer contains an alloy of the metals of the outermost layers which sandwich it. The structure is achieved by preparing two different paste layers, each of which contains a metal, glass frit and an organic vehicle (column 7 lines 65-68 column 8 lines 34-36). The two paste layers are sequentially coated and dried on the device body 12 (column 10 line 63 to column 11 line 8), binder is removed (column 11 lines 35-37) and the resulting pair of coating layers are co-baked (column 11 lines 28-30). The simultaneous baking results in the formation of the innermost and outermost layers of the external electrode and simultaneously forms an intermediate layer containing an alloy of the metals in the two paste compositions (column 11 lines 38-45).

In contrast to the Yoshii patent, the device of the present invention has external electrodes in which the innermost layer is a sintered layer with oxides exposed at the surface portions distant from the underlying ceramic element, the exposed oxide surface having a metal which is an electroplating seed and the intermediate layer in the present invention is an electro-plated layer obtained by taking advantage of the exposed electroplating seed in the innermost layer. Thus, both the innermost electrode layer and the intermediate electrode layer of the present invention are different from Yoshii.

It will be appreciated that the procedure in Yoshii makes it impossible to obtain the innermost and intermediary layers of the present invention. In Yoshii, the simultaneous baking of the dried paste result in sintering the metals in the respective paste. As a result, there is never an interior sintered electrode layer which is capable of having a layer electroplated thereon. The innermost layer of Yoshii, when sintered, is always covered by the intermediary layer and the exterior layer. In addition, the intermediary layer in Yoshii is obtained during the simultaneous baking and not by electroplating.

The only description of any plated layer in Yoshii is in the description of the related art where it is indicated that a tin containing plating is formed on the outermost layer of external electrodes in order to improve the bonding strength of the capacitor and solderability. That description further indicates that the plating is undesirable because it oxidizes faster in a high temperature, high humidity environment resulting in an increase in electrical resistance and a higher dielectric loss and, with repeated heat cycles, formation of microcracks which degrade the bonding to a circuit board to the extent where, sometimes the electronic component separates from that circuit board. Yoshii thus desires to avoid the plating on the exterior surface of the external electrodes of the prior art.

As is apparent from the foregoing discussion, Yoshii does not teach or suggest the claimed invention nor does it make the invention obvious. Accordingly, withdrawal of the rejection is respectfully solicited.

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Respectfully submitted,

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